Meeting #5

Drawing out a simplified version of our potential data path, to determine a RTL.

We have agreed on multi-cycle for our processor, one main reason being we will be using the common *swap* frequently when writing assembly code, multi-cycle should make these swaps take hardly anytime.

Li and lui are going to be hard wired in, saves one instruction for our design.

Copy and move are going to be hard wired and swap will a pseudo instruction.

RTL

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Instruction Fetch -> IR = Mem[PC]

PC = PC + 1

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Instruction Decode -> ALUinA = Reg[$m]

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Register Fetch -> ALUinB = Reg[IR[11:0]]

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Exection -> ALUout = AiA op BiB

Mem Access Reg[0] = ALUout